# Lab 2 Behavioral Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? \_yes\_\_

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here. Otherwise write “n/a”: **\_\_n/a\_\_**

Student Name: Chris Cyr  
Student ID: 12436037  
Date Completed: 5/2/22  
Time Spent: Reviewing Digital Design Material: 1 hour  
 Design/Preparation Work: 1 hour  
 VHDL Coding & Debugging: 1 hour

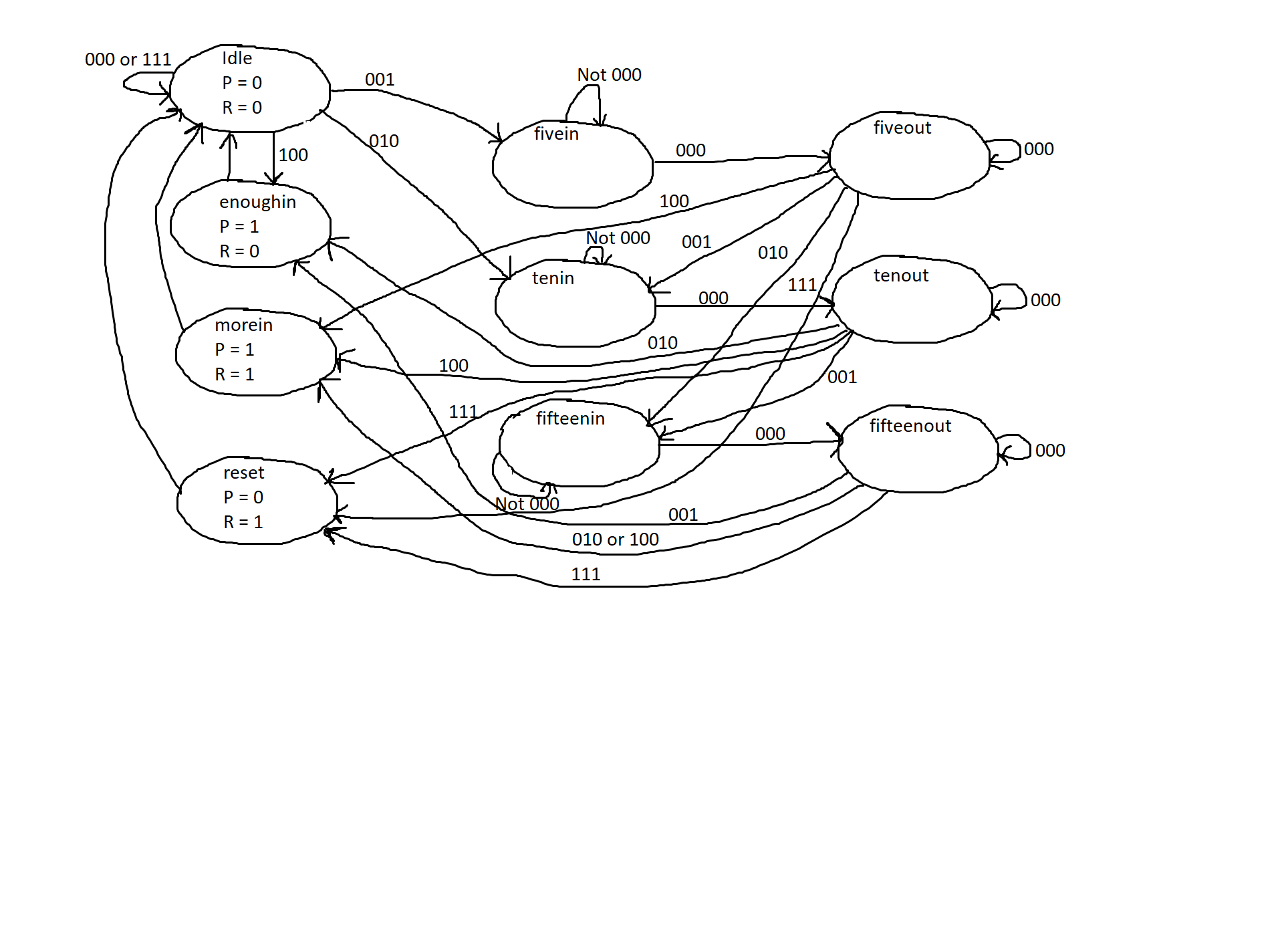
## Behavioral Overview

What % do you feel you completed on the lab? Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

\_\_100%\_\_

## Lab 2 FSM

Show your FSM for Lab 2 here. You can use Visio, another UML Diagramming tool, or attach a picture of your FSM as long as it is legible.



## Lab 2 Behavioral Simulation Graph

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

A screenshot of a computer

Description automatically generated with medium confidence